REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1-28 remain pending. Claims 1-28 have been rejected.

Claims 1, 6, 7, 13, 19, and 25 have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

REJECTIONS UNDER 35 U.S.C. § 112

Claim 6 has been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants have amended claim 2 to overcome the Examiner's rejection.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 3-7, 9-13, 16, 19, 20, 25, 27 and 28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,792,481 to Hoang, et al. ("Hoang") in view of U.S. Patent No. 6,418,489 to Mason, et al. ("Mason").

Applicants have amended claim 1 to include writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate the position in the buffer.

Hoang discloses the direct memory access (DMA) controller coupled to the processor and memory by the bus (Figure 1, col. 2, lines 19-38). More specifically, Hoang discloses

> Shown in FIG. 2 is DMA controller 20 of FIG. 1 in more detail. Also shown in FIG. 2 are FIFO 26, FIFO 24, bus 11, CODEC 28, and CODEC 30. DMA controller 20 has a receiving portion 42 and a sending portion 44. Receiving portion 42 comprises a buffer start address 50, a buffer end address 52, an interrupt period 54, a DMA control state

machine 56, a buffer current position 58, an interrupt counter 60, and a missing sample counter 62.

(Hoang, col. 3, lines 57-63, Figure 2) (emphasis added)

Further, Hoang discloses

Similar to receiving portion 42, sending portion 44 comprises a buffer start address 70, a buffer end address 72, an interrupt period 74, a DMA control state machine 76, a buffer current position 78, an interrupt counter 80, and a missing sample counter 82.

(Hoang, col. 4, lines 57-63, Figure 2) (emphasis added)

In particular, Hoang discloses

Upon initialization, the DMA control state machines 56 and 76 set buffer current positions 58 and 78 to the starting address in buffer start addresses 50 and 70. Buffer current positions 58 and 78 are updated on every successful transfer.

(Hoang, col. 4, lines 28-32) (emphasis added)

Thus, Hoang merely discloses updating buffer current positions registers that are located in the DMA controller. In contrast, amended claim 1 refers to writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate the position in the buffer.

It is respectfully submitted that Hoang does not teach or suggest a combination with Mason, and Mason does not teach or suggest a combination with Hoang. Hoang teaches a DMA controller that counts a number of missing samples when the bus is occupied by another device. Mason, in contrast, teaches the DMA controller that directly executes a plurality of tasks (Abstract). It would be impermissible hindsight, based on Applicants' own disclosure, to combine Hoang and Mason.

Furthermore, even if Hoang and Mason were combined, such a combination would lack

writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate the position in the buffer, as recited in amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Hoang in view of Mason.

Because claims 3-7, 9-13, 16, 19, 20, 25, 27 and 28 contain related limitations, Applicants respectfully submit that claims 3-7, 9-13, 16, 19, 20, 25, 27 and 28 are not obvious under 35 U.S.C. § 103(a) over Hoang in view of Mason.

Claims 2, 8, 14, 17, 18, 23 and 24 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hoang in view of Mason and further in view of Applicant's Admitted Prior Art ("AAPA"). Applicants reserve the right to challenge whether the identified teaching qualifies as AAPA.

As set forth above, neither Hoang, Mason, AAPA, nor any combination thereof discloses, teaches, or suggests writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate the position in the buffer, as recited in amended claim 1.

Because claims 2, 8, 14, 17, 18, 23 and 24 contain the related limitations, Applicants respectfully submit that claims 2, 8, 14, 17, 18, 23 and 24 are not obvious under 35 U.S.C. § 103(a) over Hoang in view of Mason, and further in view of AAPA.

Claims 15, 21, 22 and 26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hoang in view of Mason and further in view of U.S. Patent No. 6,693,753 to Su, et al. ("Su").

It is respectfully submitted that Hoang does not teach or suggest a combination with Mason and Su. Mason does not teach or suggest a combination with Hoang and Su, and Su does not teach or suggest a combination with Hoang and Mason. Hoang teaches a DMA controller

that counts missing samples when the bus is occupied by another device. Mason, in contrast, teaches the DMA controller that directly executes a plurality of tasks (Abstract). Su, in contrast to Mason and Hoang, discloses a disk sequencer supporting pipelined and non-pipelined read (Abstract). It would be impermissible hindsight, based on Applicants' own disclosure, to combine Hoang, Mason, and Su.

Furthermore, even if Hoang, Mason, and Su were combined, such a combination would lack writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate the position in the buffer, as recited in amended claim 1.

Because claims 15, 21, 22 and 26 contain the related limitations, Applicants respectfully submit that claims 15, 21, 22 and 26 are not obvious under 35 U.S.C. § 103(a) over Hoang in view of Mason, and further in view of Su.

CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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